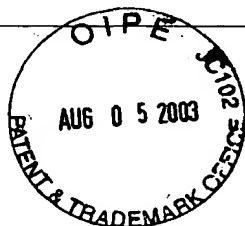


**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:  
Yuichi SATO

Application No.: 09/412,328

Filed: October 5, 1999



Group Art Unit: 2814

Examiner: D. Wille

For: STATIC RANDOM ACCESS MEMORY  
AND SEMICONDUCTOR DEVICE USING  
MOS TRANSISTORS HAVING CHANNEL  
REGION ELECTRICALLY CONNECTED  
WITH GATE

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT****Mail Stop DD**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

In accordance with 37 CFR 1.97, Applicant(s) hereby make of record the following additional documents. A PTO Form SB/08 and a full copy of each of these documents accompany this statement.

Applicant(s) have become aware of certain documents, cited in a Japanese Patent Office Official Action issued September 3, 2002, during the prosecution of Japanese application no. JP293047, which corresponds to the above referenced application, and in accordance with 37 CFR 1.97(c) and (e)(1) or (b)(3), hereby submit(s) these documents for the Examiner's consideration. These documents are cited on the enclosed PTO Form SB/08, and a copy of the JPO Official Action and each document cited thereon are enclosed as well.

Applicants have also become aware of further documents cited in a Korean Patent Office Official Action dated June 9, 2003, during the prosecution of Korean application no. 021436500, which also corresponds to the above referenced application, and in accordance with 37 CFR 1.97(c) and (e)(1) or (b)(3), hereby submit(s) these documents for the Examiner's consideration. These documents are cited on the enclosed PTO Form SB/08, and a copy of the KPO Official Action and each document cited thereon are enclosed as well.

08/06/2003 DTESSEM1 00000146 031952 09412328

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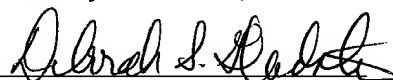
va-40662

The undersigned hereby certifies that some items contained in this Supplemental Information Disclosure Statement were cited in a communication from a foreign patent office in a counterpart foreign application more than three months prior to the filing of this statement. Therefore, a fee is due. A fee transmittal is included with this document.

This statement is not to be interpreted as a representation that the cited documents are material, that an exhaustive search has been conducted, or that no other relevant information exists. Nor shall the citation of any document herein be construed *per se* as a representation that such document is prior art. Moreover, Applicant(s) understand(s) the Examiner will make an independent evaluation of the cited documents.

Dated: August 5, 2003

Respectfully submitted,

By   
Deborah S. Gladstein

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McLean, Virginia 22102  
(703) 760-7753  
Attorneys for Applicant

Form PTO-1449

Docket Number 204552016500

Application Number 09/412,328

INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION

Applicant

Yuichi SATO

Filing Date October 5, 1999

Group Art Unit 2814

Mailing Date August 5, 2003

(On several sheets if necessary)

## U.S. PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate

## FOREIGN PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES NO
	1.	3/1979	JP-A-54-037544	Japan			abs.
	2.	8/1986	JP-A-61-185972	Japan			abs.
	3.	1/1991	JP3022476	Japan			abs.
	4.	2/1992	JP-A-04-053090	Japan			abs.
	5.	6/1995	JP-A-07-161844	Japan			abs.
	6.	5/1996	JP-A-07-176633	Japan			abs.
	7.	8/1998	JP-A-10-222985	Japan			abs.

## OTHER DOCUMENTS

(including author, title, Date, Pertinent Pages, Etc.)

Examiner Initials	Ref. No.	Title
	8.	F. Assaderaghi et al., "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI", IEEE Transactions on Electron Devices, vol. 44, no. 3, pp. 414-422, March 1997

EXAMINER:

1DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.